

CLAIMS

What is claimed is:

- 1 1. A single integrated circuit comprising
2 a plurality of logic elements (LEs) for generating a plurality of output signals in
3 response to a plurality of input signals correspondingly applied to the LEs, each of
4 the LEs being equipped to hold constant the LE's output signal on demand; and
5 a context bus, including associated read/write control facilities, coupled to the
6 LEs for outputting individual signal state values of the LEs out of the integrated
7 circuit, and for initializing the LEs with individual signal state values provided to the
8 integrated circuit while the output signals of the LEs are being held constant.

- 1 2. The integrated circuit as set forth in claim 1, wherein the integrated circuit
2 further comprises a scan register coupled to the LEs for serially capturing and
3 outputting a trace record of all signal state values of the LEs in a particular clock
4 cycle of an operating clock outside the integrated circuit, the scan register being
5 provided with a scan clock appropriately scaled to the operating clock.

- 1 3. The integrated circuit as set forth in claim 1, wherein the integrated circuit
2 further comprises trigger circuitry coupled to the LEs for conditionally generating at
3 least one trigger value depending on the signal state values of the LEs.

- 1 4. The integrated circuit as set forth in claim 3, wherein the trigger circuitry
2 comprises
3 a first register for storing a first trigger pattern; and

4 a first comparator coupled to the LEs and the first register for conditionally
5 generating a first trigger value if signal state values of the LEs match the stored first
6 trigger pattern.

1 5. The integrated circuit as set forth in claim 1, wherein
2 each LE further includes a multiple input-single output truth table for
3 generating a first intermediate output signal in response to a first set of input signals;
4 a first selector coupled to the truth table and the context bus for selecting
5 either the first intermediate output signal, the output of the LE feedback to the first
6 selector, or a predesignated bus signal on the context bus, and outputting the
7 selected signal; and
8 a first control circuit coupled to the first selector for controlling the first
9 selector.

1 6. The integrated circuit as set forth in claims 5, wherein each LE further
2 comprises
3 a pair of master-slave latches, each having a data input, a set input, and a
4 reset input, coupled to the first selector for generating a second and a third
5 intermediate output signal in response to the data, set, and reset inputs, the
6 selected and third intermediate output signals being provided as data inputs to the
7 master and slave latches respectively;
8 a second control circuit coupled to the pair of master-slave latches for
9 providing each of the master and slave latches with a set and a reset value; and
10 a second selector coupled to the truth table and the master-slave latches for
11 selecting either the first, second or third intermediate output signal as the output
12 signal of the LE.

1 7. The integrated circuit as set forth in claim 6, wherein each LE further
2 comprises a buffer coupled to the second selector for outputting the output signal of
3 the LE onto the context bus.

1 8. The integrated circuit as set forth in claim 6, wherein the second control
2 circuit comprises a first and a second AND gate for receiving a first and a second
3 plurality of input control signals, and in response, generating the set and reset
4 values for the master and slave latches respectively.

1 9. The integrated circuit as set forth in claim 6, wherein the LE further comprises
2 a third selector for selectively providing either an emulation clock or a debugging
3 clock to the master and slave latches.

1 10. The integrated circuit as set forth in claim 9, wherein the LE further comprises
2 a fourth and a fifth selector for selectively providing one of a plurality of clocks to the
3 third selector as the emulation clock.

1 11. The integrated circuit as set forth in claim 5, wherein the first control circuit
2 comprises an OR gate and an AND gate serially coupled to the OR gate for
3 receiving a plurality of input control signals, and in response, generating an output
4 control signal for causing the first selector to select the output signal of the LE
5 feedback to the first selector.

1 12. The integrated circuit as set forth in claim 5, wherein the first control circuit
2 comprises a NOR gate for receiving a plurality of input control signals, and in
3 response generating an output control signal for causing the first selector to select
4 the first intermediate output signal.

1 13. The integrated circuit as set forth in claim 5, wherein the control circuit
2 receives a load control signal, and in response, output the load control signal for the
3 first selector for causing the first selector to select the predesignated bus signal on
4 the context bus.

1 14. A single integrated circuit comprising a plurality of logic elements (LEs) for
2 generating a plurality of output signals in response to a plurality of input signals
3 correspondingly applied to the LEs, and a scan register coupled to the LEs for
4 serially capturing and outputting a trace record of all signal state values of the LEs in
5 a particular clock cycle of an operating clock outside the integrated circuit, the scan
6 register being provided with a scan clock appropriately scaled to the operating clock.

1 15. The integrated circuit as set forth in claim 14, wherein the integrated circuit
2 further comprises trigger circuitry coupled to the LEs for conditionally generating at
3 least one trigger value depending on the signal state values of the LEs.

1 16. The integrated circuit as set forth in claim 15, wherein the trigger circuitry
2 comprises
3 a first register for storing a first trigger pattern; and
4 a first comparator coupled to the LEs the first register for conditionally
5 generating a first trigger value if signal state values of the LEs match the stored first
6 trigger pattern.

1 17. The integrated circuit as set forth in claim 14, wherein
2 each LE further includes a multiple input-single output truth table for
3 generating a first intermediate output signal in response to a first set of input signals;

4 a first selector coupled to the truth table and the context bus for selecting
5 either the first intermediate output signal, or the output of the LE feedback to the first
6 selector, and outputting the selected signal; and
7 a first control circuit coupled to the first selector for controlling the first
8 selector.

1 18. The integrated circuit as set forth in claims 17, wherein each LE further
2 comprises

3 a pair of master-slave latches, each having a data input, a set input, and a
4 reset input, coupled to the first selector for generating a second and a third
5 intermediate output signal in response to the data, set, and reset inputs, the
6 selected and third intermediate output signals being provided as data inputs to the
7 master and slave latches respectively;

8 a second control circuit coupled to the pair of master-slave latches for
9 providing each of the master and slave latches with a set and a reset value; and

10 a second selector coupled to the truth table and the master-slave latches for
11 selecting either the first, second or third intermediate output signal as the output
12 signal of the LE.

1 19. The integrated circuit as set forth in claim 18, wherein the LE further
2 comprises a third selector for selectively providing either an emulation clock or a
3 debugging clock to the master and slave latches.

1 20. A single integrated circuit comprising a plurality of logic elements (LEs) for
2 generating a plurality of output signals in response to a plurality of input signals
3 correspondingly applied to the LEs, and trigger circuitry coupled to the LEs for

4 conditionally generating at least one trigger value depending on the signal state
5 values of the LEs.

1 21. The integrated circuit as set forth in claim 20, wherein the trigger circuitry
2 comprises
3 a first register for storing a first trigger pattern; and
4 a first comparator coupled to the LEs the first register for conditionally
5 generating a first trigger value if signal state values of the LEs match the stored first
6 trigger pattern.

1 22. The integrated circuit as set forth in claim 20, wherein
2 each LE further includes a multiple input-single output truth table for
3 generating a first intermediate output signal in response to a first set of input signals;
4 a first selector coupled to the truth table and the context bus for selecting
5 either the first intermediate output signal, or the output of the LE feedback to the first
6 selector, and outputting the selected signal; and
7 a first control circuit coupled to the first selector for controlling the first
8 selector.

1 23. The integrated circuit as set forth in claims 22, wherein each LE further
2 comprises
3 a pair of master-slave latches, each having a data input, a set input, and a
4 reset input, coupled to the first selector for generating a second and a third
5 intermediate output signal in response to the data, set, and reset inputs, the
6 selected and third intermediate output signals being provided as data inputs to the
7 master and slave latches respectively;

8 a second control circuit coupled to the pair of master-slave latches for
9 providing each of the master and slave latches with a set and a reset value; and
10 a second selector coupled to the truth table and the master-slave latches for
11 selecting either the first, second or third intermediate output signal as the output
12 signal of the LE.

1 24. The integrated circuit as set forth in claim 23, wherein the LE further
2 comprises a third selector for selectively providing either an emulation clock or a
3 debugging clock to the master and slave latches.

1 25. A single integrated circuit comprising a plurality of logic elements (LEs) for
2 generating a plurality of output signals in response to a plurality of input signals
3 correspondingly applied to the LEs, each LE includes
4 a multiple input-single output truth table for generating a first intermediate
5 output signal in response to a first set of input signals;
6 a first selector coupled to the truth table and the context bus for selecting
7 either the first intermediate output signal, or the output of the LE feedback to the first
8 selector, and outputting the selected signal; and
9 a first control circuit coupled to the first selector for controlling the first
10 selector.

1 26. The integrated circuit as set forth in claims 25, wherein each LE further
2 comprises
3 a pair of master-slave latches, each having a data input, a set input, and a
4 reset input, coupled to the first selector for generating a second and a third
5 intermediate output signal in response to the data, set, and reset inputs, the

6 selected and third intermediate output signals being provided as data inputs to the
7 master and slave latches respectively;

8 a second control circuit coupled to the pair of master-slave latches for
9 providing each of the master and slave latches with a set and a reset value; and
10 a second selector coupled to the truth table and the master-slave latches for
11 selecting either the first, second or third intermediate output signal as the output
12 signal of the LE.

1 27. The integrated circuit as set forth in claim 26, wherein the LE further
2 comprises a third selector for selectively providing either an emulation clock or a
3 debugging clock to the master and slave latches.